IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) Process for testing an integrated circuit comprising memory points ~~(140)~~ and a Boundary Scan chain ~~(120)~~, in which one writes and/or reads to and/or from the memory points ~~(140)~~ by way of an access path ~~(150)~~ to the memory points ~~(140)~~ from an outside terminal ~~(108)~~ of the circuit, comprising: ~~characterized in that~~

activating the Boundary Scan chain ~~(120) is activated~~ so as to impose and/or observe logic levels on the inputs/outputs ~~(110)~~ of the integrated circuit.

2. (Currently Amended) Process according to claim 1, characterized in that the access path ~~(150)~~ to the memory points ~~(140)~~ and the Boundary Scan chain ~~(120)~~ are activated simultaneously.

3. (Currently Amended) Process according to claim 1 or 2, characterized in that the access path (ISO) to the memory points ~~(140)~~ and the Boundary Scan chain are activated by way of a line comprising in series the access path ~~(150)~~ to the memory points ~~(140)~~ and the Boundary Scan chain ~~(120)~~.

4. (Currently Amended) Process according to ~~any one of claims 1 to 3~~claim 1 or claim 2, characterized in that the Boundary Scan chain ~~(120)~~ is activated by way of an activation path ~~(150)~~ linked to the Boundary Scan chain ~~(120)~~ downstream of a TAP controller ~~(200)~~.

5. (Currently Amended) Process according to claim 4, characterized in that the activation path ~~(150)~~ is linked to the Boundary Scan chain ~~(120)~~ at least by a logic gate ~~(210, 220, 230, 240, 250)~~ able to link, as a function of a control signal (ATPG-mode), the Boundary Scan chain ~~(120)~~ or else to the activation path ~~(150)~~ of the Boundary Scan, or else to the TAP controller ~~(200)~~.

6. (Currently Amended) Process according to ~~either of claims 4 and 5~~claim 4, characterized in that the activation path ~~(150)~~ includes at least one channel (ATPG-Si) on which is placed at least one memory point ~~(140)~~ , this channel being able to be linked in series with the Boundary Scan chain ~~(120)~~ when the latter is activated.

7. (Currently Amended) Process according to ~~one of the preceding claims~~claim 1 or claim 2, characterized in that the input channel (Si). clock channel (ck) and configuration channel (Sh) of the Boundary Scan chain ~~(120)~~ are linked to logic gates ~~(210, 220, 230, 240, 250)~~ which are able to link, according to a control signal (ATPG-mode), these channels (Si, ck, Sh) or else to the input channel (Si), clock channel (ck) and configuration channel (Sh) of the TAP controller ~~(200)~~ or else to the input channel (Si), clock channel (ck) and configuration channel (Sh) of the activation path ~~(150)~~.

8. (Currently Amended) Process according to ~~one of the preceding claims~~claim 1 or claim 2, characterized in that all the memory points ~~(140)~~ are linked in series.

9. (Currently Amended) Process according to ~~one of the preceding claims~~claim 1 or claim 2, characterized in that at least some of the inputs/outputs ~~(100)~~ of the integrated circuit are connected directly to a tester able to inject chosen signals directly into certain of these inputs/outputs ~~(100)~~, and/or to receive output signals directly from certain of these inputs/outputs ~~(100)~~ and to compare these output signals with expected signals.

10. (Currently Amended) Process according to ~~one of the preceding claims in combination with~~ claim 1, claim 2 or claim 9, characterized in that the injection and/or direct measurement tester is coordinated with a device for controlling the Boundary Scan chin ~~(120)~~ so as to generate test vectors on sets comprising both inputs/outputs ~~(103)~~ connected directly to the tester and also inputs/outputs ~~(105)~~ connected to the tester via the Boundary Scan chain ~~(120)~~.

11. (Currently Amended) Process according to ~~one of the preceding claims~~claim 1 or claim 2, characterized in that the circuit comprises accesses ~~(150)~~ to its set of memory points ~~(140)~~ and in that the test is carried out by controlling the set of memory points ~~(140)~~ so that the function of the integrated circuit is reduced to a combinatorial function.

12. (Currently Amended) Integrated circuit comprising a Boundary Scan chain ~~(120)~~ and an access path ~~(150)~~ to at least one memory point ~~(140)~~, characterized in that the access path ~~(150)~~ and the Boundary Scan chain ~~(120)~~ are linked in series and in that the circuit comprises means ~~(220, 230, 240, 250)~~ for intervening simultaneously on the memory point or points ~~(140)~~ of the access path ~~(150)~~ and on the cells ~~(110)~~ of the Boundary Scan chain ~~(120)~~.

13. (Currently Amended) Integrated circuit according to claim 12, characterized in that the means ~~(220, 230, 240, 250)~~ for intervening simultaneously on the memory point or points ~~(140)~~ of the access path ~~(150)~~ and on the cells ~~(110)~~ of the Boundary Scan chain ~~(120)~~ comprise at least one logic gate ~~(220, 230, 240, 250)~~ able to link the Boundary Scan chain ~~(120)~~ or else to the access path ~~(150)~~, or else to a TAP controller ~~(200)~~.

14. (Currently Amended) Integrated circuit according to claim 12 or claim 13, characterized in that the input channel (Si), clock channel (CM) and configuration channel (SHIFT) of the Boundary Scan chain ~~(120)~~ are linked to logic gates ~~(220, 230, 240, 250)~~ which are able to link, according to a control signal (MODE), these channels or else to the input channel (ST), clock channel (CM) and configuration channel (SHIFT) of the TAP controller ~~(200)~~, or else to the input channel (ATPG_si), clock channel (ATPG_ck) and configuration channel (ATPQ_se) of the access path ~~(150)~~.

15. (Currently Amended) Integrated circuit according to ~~one of claims 12 to 14~~claim 12 or claim 13, characterized in that all the memory points ~~(140)~~ of the integrated circuit are linked in series.

16 – 21 (Canceled)

22. (New) Integrated circuit tester, comprising:

a first module means for imposing and/or reading states of memory points of an integrated circuit,

a second module means for imposing states and/or reading states of input/output cells by way of the Boundary Scan chain of the circuit simultaneously with the action of the first module.

23. (New) Integrated circuit tester according to claim 22, comprising means for simultaneously injecting into an integrated circuit, control signals (SI) for the memory points and control signals (SI) for the inputs/outputs of the Boundary Scan.

24. (New) Tester according to claim 22, comprising means for injecting the control signals for the memory points and the control signals for the inputs/outputs of the Boundary Scan onto one and the same channel.

25. (New) Tester according to claims 22 to 24, comprising:

a series of channels coupled directly to inputs/outputs of an integrated circuit, and

a module means for injecting chosen signals directly into certain of the inputs /outputs, and/or to receive output signals from the inputs/outputs so as to compare the output signals with expected signals.

26. (New) Tester according to claim 25, comprising:

a control device for the Boundary Scan chain of an integrated circuit coordinated with the direct injection/reception module so as to generate test vectors on sets comprising both inputs/outputs connected directly to the tester and also inputs/outputs connected to the tester via the Boundary Scan chain.

27. (New) Tester according to one of claims 22 to 24, comprising means for controlling the set of memory points in such a way that the function of the integrated circuit is reduced to a combinatorial function during the test.